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(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Sakaino et al.

Batch No.:

Application No.: 09/229,628

Allowed: July 27, 2004

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Art Unit: N/A

For: SEMICONDUCTOR INTEGRATED CIRCUIT

Examiner: Not Yet Assigned

SUBMISSION OF FORMAL DRAWINGS

MS PGPUB Drawings Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Dear Sir:

Submitted herewith is one set (six sheets, six figures) of formal drawings for filing in the above-identified Patent application. Kindly substitute the enclosed formal drawings for the informal drawings submitted with the originally filed application.

Dated: September 29, 2004

Respectfully submitted

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